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09/988,939	11/21/2001	Tom Davis	A363 0015	9159

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EXAMINER	
MATTIS, JASON E	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,939	DAVIS ET AL.	
	Examiner	Art Unit	
	Jason E Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 November 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/25/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "11" has been used to designate both an ingress in Figure 1 and a packet in Figure 1. As described in page 8 paragraph 20 of the specification, the packet should be correctly labeled as item "13" not item "11". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 8-16, 19-21, and 24-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Paatela et al. (U.S. Pub. US 2002/0163935 A1).

With respect to claim 1, Paatela et al. discloses a method for packet processing **(See page 4 paragraph 48 and Figures 3 and 17 of Paatela et al. for reference to an ingress processing system 300 that performs a method as shown in Figure 17)**. Paatela et al. also discloses obtaining first information regarding a packet and using the first information as an index into a parser memory **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to pre-processor 310 performing a packet protocol identification, which is obtaining first information, and for reference to using the protocol information to obtain a protocol layer code, which is an index to a CAM, which is a parser memory)**. Paatela et al. further discloses retrieving from the parser memory an entry comprising a location in the packet of one or more protocol bits specifying a protocol associated with the packet **(See page 4 paragraph 51 and Figure 3 of Paatela et al. for reference to using the protocol layer code to access an instruction memory with pointers to access selected words in the packet)**. Paatela et al. also discloses obtaining a match engine index **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to the parsing engine 312 using the selected words as keys to obtain search result information, which is a match engine index)**. Paatela et al. further discloses using

the protocol bits and the match engine index as a key to retrieve a match engine entry from a match engine memory, with the match engine entry comprising an action to take on the packet **(See pages 5-6 paragraph 59-63 and Figure 7 of Paatela et al. for reference to using search results to retrieve instructions, which are match engine entries, from a memory 703, which is a match engine memory, with the instructions comprising an action to take on the packet)**. .

With respect to claim 2, Paatela et al. discloses that the match engine index is included in the parser memory entry **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to the search results being obtained from CAM)**.

With respect to claim 3, Paatela et al. discloses that the parser memory entry comprises a context memory base address and either a location in the packet of a set of label bits or an indication that there are no label bits **(See page 4 paragraph 51 of Paatela et al. for reference to the memory entry including pointers to selected words of the packet)**. Paatela et al. also discloses that if the parser memory includes a location of a set of label bits, retrieving from the packet the label bits and obtaining the match engine index using the context memory base address and label bits to retrieve from a context memory an entry comprising a match engine index **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to using the selected words to build a search key that is applied against a CAM to generate the search results, which are the match engine indices, from the CAM)**.

With respect to claim 4, Paatela et al. discloses that if the location in the packet indicates that there are no label bits, obtaining the match engine index included in the parser memory entry **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to the search results being obtained from CAM)**.

With respect to claim 8, Paatela et al. discloses that obtaining the first information comprises identifying a channel with which the packet is associated **(See page 3 paragraph 42 of Paatela et al. for reference to the packet classification being based on the route/flow of the packet, which is a channel that the packet is associated with)**.

With respect to claim 9, Paatela et al. discloses a method for packet processing in a packet processing system **(See page 4 paragraph 48 and Figures 3 and 17 of Paatela et al. for reference to an ingress processing system 300 that performs a method as shown in Figure 17)**. Paatela et al. also discloses obtaining first information regarding a packet and retrieving an entry corresponding to the first information from a parser memory **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to pre-processor 310 performing a packet protocol identification, which is obtaining first information, and for reference to using the protocol information to obtain a protocol layer code, which is an index to a CAM, which is a parser memory)**. Paatela et al. further discloses retrieving from the packet one or more protocol bits identified by the parser memory entry **(See page 4 paragraph 51 and Figure 3 of Paatela et al. for reference to using the protocol layer code to access an instruction memory with pointers to access selected words in the**

packet). Paatela et al. also discloses retrieving from a match engine memory a match engine memory entry comprising an action to perform using a match engine key comprising a combination of the protocol bits and a match engine index **(See page 4 paragraph 51, page 5 paragraph 55, pages 5-6 paragraphs 59-63 and Figures 3-4 and 7 of Paatela et al. for reference to the parsing engine 312 using the selected words as keys to obtain search result information, which is a match engine index and for reference to using search results to retrieve instructions, which are match engine entries, from a memory 703, which is a match engine memory, with the instructions comprising an action to take on the packet)**. Paatela et al. further discloses performing the action specified in the retrieved match engine entry **(See pages 5-6 paragraphs 59-63 of Paatela et al. for reference to the editing system 700 performing the action specified by the retrieved instruction)**.

With respect to claim 10, Paatela et al. discloses extracting information relating to another protocol from the packet **(See page 5 paragraph 53 of Paatela et al. for reference to performing protocol transformations on a packet, meaning the packet has protocol information extracted and replaced with new protocol information)**.

With respect to claim 11, Paatela et al. discloses that an action is selected from forwarding the packet, discarding the packet, adding additional header information to the packet, associating the packet with a quality of service level, and extracting information relating the another protocol from the packet **(See pages 5-6 paragraph 52-53 and 68 of Paatela et al. for reference to instructions including dropping the**

packet, steering, or forwarding, the packet, modifying the packet by adding header information, associating the packet with a policed flow rate, which is a quality of service, and performing protocol transformations on a packet, meaning the packet has protocol information extracted and replaced with new protocol information).

With respect to claim 12, Paatela et al. discloses a packet processing apparatus **(See page 4 paragraph 48 and Figure 3 of Paatela et al. for reference to an ingress processing system 300).** Paatela et al. also discloses a control logic circuit **(See pages 4-5 paragraphs 48-53 and Figure 3 of Paatela et al. for reference to pre-processor 310, parsing engine 312, policing engine 313 and editor 314, which together comprise the control logic circuitry of the processing system 300).** Paatela et al. further discloses a parser memory accessible to the control logic circuit and comprising a plurality of entries each specifying a locating in a packet of one or more protocol bits and at least some of which specifying match engine index **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to a content-addressable memory, which is a parser memory, that contains both protocol layer code information, which specifies pointers to selected packet words, and search results, which are match engine indices).** Paatela et al. also discloses a match engine memory accessible to the control logic circuit, with the match engine memory comprising a plurality of entries each specifying an action to be taken **(See page 5 paragraph 61 and Figure 7 of Paatela et al. for reference to memory 703, which is a memory comprising instructions, which are actions to be taken).** Paatela et al.

further discloses a context memory accessible to the control logic circuit comprising a plurality of entries each specifying a match engine index **(See page 4 paragraph 51 for reference to a CAM storing search results, which are match engine indices)**. Paatela et al. also discloses generating a match engine key by combining protocol bits of a packet identified in a parser memory with a match engine index from an entry of the parser memory of the context memory **(See page 4 paragraph 51, page 5 paragraph 55, and Figure 4 of Paatela et al. for reference to using selected words from the packet and information retrieved from the CAM to generate search results, which are match engine indices)**. Paatela et al. further discloses retrieving from the match engine memory an entry corresponding to the match engine key and performing an action specified in the match engine entry **(See pages 5-6 paragraphs 61-63 and Figure 7 of Paatela et al. for reference to using search results to retrieve instructions, which is a match engine memory entry, and performing the instructions of the packet)**.

With respect to claims 13, 14, 15, and 16, Paatela et al. discloses that the control logic circuit comprises an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contains an interface to the external memory **(See page 5 paragraphs 57-58 and Figures 5-6 of Paatela et al. for reference to the components of the control logic circuit being included on a single integrated circuit with the memories and buffers optionally being either incorporated into the common chip or external to the common chip, with the common chip including interfaces to an external memory)**.

With respect to claim 19, Paatela et al. discloses that the control logic circuit comprises a pipelined architecture **(See Figure 3 of Paatela et al. for reference to the pipelined architecture of the elements 310, 312, 313, and 314 that make up the control logic circuit)**.

With respect to claim 20, Paatela et al. discloses a configurable device for processing packets supporting plurality of protocols **(See page 4 paragraph 48 and Figure 3 of Paatela et al. for reference to an ingress processing system 300 that supports multiple protocols)**. Paatela et al. also discloses a first internal memory **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to a content-addressable memory, which is a first internal memory)**. Paatela et al. further discloses a second internal memory comprising a plurality of entries comprising an action to be taken on the packet **(See page 5 paragraph 61 and Figure 7 of Paatela et al. for reference to memory 703, which is a memory comprising instructions, which are actions to be taken)**. Paatela et al. also discloses logic circuitry for identifying a channel value associated with the packet, retrieving an entry from the first memory using the channel value as an index and obtaining an entry address information identifying a set of entries in external context memory applicable to the channel value **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to pre-processor 310 and parsing engine 312, which are logic circuitry that identify a protocol layer code, which is an address identifying an entry in a CAM, based on a packet type classified on the basis of packet flow, or channel)**. Paatela et al. further discloses logic circuitry for using the address information and one

or more bits from the packet to retrieve from the external context memory one entry **(See page 4 paragraph 51, page 5 paragraph 55, and Figures 3-4 of Paatela et al. for reference to parsing engine 312 using selected words from the packet and the protocol layer code to determine a search result, which is an entry from the CAM)**. Paatela et al. also discloses logic circuitry for using the information from the one entry to retrieve from the second memory an action to be taken on the packet **(See pages 5-6 paragraphs 61-63 and Figure 7 of Paatela et al. for reference to editing system 700 using the search result to retrieve instructions from memory 703)**.

With respect to claim 21, Paatela et al. discloses that the action to be taken comprises extracting information relating to a protocol from the packet **(See page 5 paragraph 53 of Paatela et al. for reference to performing protocol transformations on a packet, meaning the packet has protocol information extracted and replaced with new protocol information)**.

With respect to claim 24, Paatela et al. discloses a packet processing device **(See page 4 paragraph 48 and Figure 3 of Paatela et al. for reference to an ingress processing system 300)**. Paatela et al. also discloses a means for retrieving first information about a received packet and a means for retrieving an entry corresponding to the first information **(See page 4 paragraphs 50-51 and Figure 3 of Paatela et al. for reference to pre-processor 310 performing a packet protocol identification, which is obtaining first information, and for reference to using the protocol information to obtain a protocol layer code, which is an index to a CAM, which is a parser memory)**. Paatela et al. further discloses the entry comprising a location in

the packet of one or more protocol bits specifying a protocol associated with the packet and a match engine index **(See page 4 paragraph 51 and Figure 3 of Paatela et al. for reference to using the protocol layer code to access an instruction memory with pointers to access selected words in the packet)**. Paatela et al. also discloses a means for generating a match engine key **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to the parsing engine 312 using the selected words as keys to obtain search result information, which is a match engine index)**. Paatela et al. further discloses a means for retrieving an action corresponding to a match engine entry and a means for performing the action **(See pages 5-6 paragraphs 61-63 and Figure 7 of Paatela et al. for reference to editing system 700 using the search result to retrieve instructions from memory 703 and for reference to performing the instructions on the packet)**.

With respect to claim 25, Paatela et al. discloses that the first information comprises an ATM channel associated with the packet **(See page 1 paragraph 9 and page 3 paragraph 42 of Paatela et al. for reference to the packet classification being based on the route/flow of the packet, which is a channel that the packet is associated with, and for reference to using ATM packets meaning the flow identified is an ATM flow)**.

With respect to claim 26, Paatela et al. discloses a means for forwarding the packet to another devices **(See page 5 paragraph 54 and Figure 3 of Paatela et al. for reference to switch fabric interface 316, which is a means to forward the packet to another device)**.

With respect to claim 27, Paatela et al. discloses a means for determining whether to retrieve and entry with the means for generating the match engine key doing so by using information in the entry from the external context memory **(See page 4 paragraph 51, page 5 paragraph 55 and Figures 3-4 of Paatela et al. for reference to the parsing engine 312 using the selected words as keys to obtain search result information from a CAM, which is a match engine index)**.

With respect to claim 28, Paatela et al. discloses incorporating the plural means on a single integrated circuit **(See page 5 paragraphs 57-58 and Figures 5-6 of Paatela et al. for reference to the circuitry being on a single integrated circuit chip)**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-7 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paatela et al. in view of Feldmeier et al. (U.S. Pat. 6289414).

With respect to claims 5-7 and 22, although Paatela et al. does disclose using content-addressable memories, Paatela et al. does not specifically disclose that the match engine memory is a ternary content-addressable memory.

With respect to claims 5-7 and 22, Feldmeier et al., in the field of communications, discloses using a ternary content-addressable memory **(See column 2 line 47 to column 3 line 29 for reference to using a ternary content-addressable memory)**. Using a ternary content-addressable memory has the advantage of being a faster memory, which can help achieve wire speed **(See column 2 line 47 to column 3 line 7 for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Feldmeier et al., to use a ternary content-addressable memory, as suggested by Feldmeier et al., with the system and method of Paatela et al., with the motivation being to use a faster memory, which can help achieve wire speed.

With respect to claim 23, Paatela et al. discloses that the first memory comprises a random access memory **(See page 4 paragraphs 50-51 for reference to using an SRAM)**.

6. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paatela et al.

With respect to claims 17-18, although Paatela et al. does not specifically disclose that the parser memory and match engine memory comprise 512 or fewer

entries, the size of the memories used in the packet processing apparatus are an obvious design choice that a user would make at the time of designing the apparatus. Choosing the exact size of the memory has the advantage of allowing the memory and memory access keys to be customized to the desired size of a user.

It would have been obvious for one of ordinary skill in the art at the time of the invention to choose the size of the memories to fit the needs of a user of the apparatus with the motivation being to allow memory and memory access keys to be customized to the desired size of a user.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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